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10/706,461	11/12/2003	Jae-Goo Lee	SAM-0270DIV	6750

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/706,461	LEE, JAE-GOO
	Examiner	Art Unit
	John C. Ingham	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/994,154.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/994,154, filed on 26 November 2001.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 19a. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: page 6 line 20 contains the sentence, "Preferably, the gate polyoxide layer prevents the silicon nitride from separating from the semiconductor substrate and has a thickness of about 50 ~ 100." There are no units of measurement included with the thickness, although angstroms (Å) are assumed. Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: page 14 line 2 contains the sentence, "In other words, the oxide layer 112a on the source and drain area 114 which is not protected by the external spacer 114a..." Item 114 is previously referred to as an external spacer, while item 104 is referred to as a source and drain area. Appropriate correction is required.

Claim Objections

5. Claim 1 is objected to because of the following informalities: the second occurrence of the phrase "semiconductor substrate" (page 16 line 7) should be preceded by the word "the" and not by the word "a". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 4, 6 and 8 are rejected under 35 U.S.C. 102(a) as being anticipated by Divakaruni et al. (US 6,727,539).

Regarding claim 1, Divakaruni discloses in Figure 4 a semiconductor substrate (202) having a multi-layered spacer, comprising: a plurality of gate electrodes (col. 3, ln. 27-28) each including a gate oxide layer (240), a gate conductive layer (221), and a capping dielectric layer (254) formed on a semiconductor substrate; a gate polyoxide layer (256) formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a predetermined portion of the semiconductor substrate; a silicon nitride layer (258) being in contact with the sidewalls of the capping dielectric layer and the gate polyoxide layer; an oxide layer (260) being in contact with the silicon nitride layer; and an external spacer (270) being in contact with the oxide layer.

Regarding claim 2, Divakaruni discloses in Figure 5 a pad (309, above item 357) formed in a region between adjacent gate electrodes having the multi-layered spacer (see column 9 lines 13-16) and being in contact with the semiconductor substrate; and an interlevel dielectric layer (col.9, ln. 21-25) formed on the pad and each gate electrode having the multi-layered spacer.

Regarding claim 4, the claim language "wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800~900°C with the injection of oxygen" describes a product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant polyoxide layer is not distinct from that of the disclosed oxide layer (256).

Regarding claim 6, the claim language "wherein the oxide layer is an oxide layer formed at a temperature of about 600~800°C using $SiCl_4$ and O_2" describes a product-by-process. Divakaruni discloses an oxide film (260) formed by TEOS, which is normally at a temperature around 700°C, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant oxide layer is not distinct from that of the disclosed oxide layer (260).

Regarding claim 8, Divakaruni discloses in Figure 4 that the external spacer (270) is formed of silicon nitride (col. 8, ln. 52).

8. Claims 1, 4, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Takahashi (US 6,642,586).

Regarding claim 1, Takahashi discloses in Figure 6D a semiconductor substrate (101) having a multi-layered spacer, comprising: a plurality of gate electrodes each including a gate oxide layer (104), a gate conductive layer (105), and a capping dielectric layer (106) formed on a semiconductor substrate; a gate polyoxide layer (110A) formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a predetermined portion of the semiconductor substrate; a silicon nitride layer (110B) being in contact with the sidewalls of the capping dielectric layer and the gate polyoxide layer; an oxide layer (110C) being in contact with the silicon nitride layer; and an external spacer (111a) being in contact with the oxide layer.

Regarding claim 4, the claim language "wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800~900°C with the injection of oxygen"

describes a product-by-process. Takahashi discloses an oxide film (110A) formed through thermal oxidation at a temperature of 800-1100°C, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant polyoxide layer is not distinct from that of the disclosed oxide layer (110A).

Regarding claim 6, the claim language "wherein the oxide layer is an oxide layer formed at a temperature of about 600~800°C using $SiCl_4$ and O_2" describes a product-by-process. Takahashi discloses an oxide (110C) formed by wet oxidation, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant oxide layer is not distinct from that of the disclosed oxide layer (110C).

9. Claims 1, 3, 4, 5, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (US 5,817,562), hereafter "Chang" ('562).

Regarding claim 1, Chang ('562) discloses in Figure 5 a semiconductor substrate (8) having a multi-layered spacer, comprising: a plurality of gate electrodes each including a gate oxide layer (14), a gate conductive layer (16), and a capping dielectric layer (18,20) formed on a semiconductor substrate; a gate polyoxide layer (24) formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a predetermined portion of the semiconductor substrate; a silicon nitride layer (26) being in contact with the sidewalls of the capping dielectric layer and the gate polyoxide layer; an oxide layer (28) being in contact with the silicon nitride layer; and an external spacer (30) being in contact with the oxide layer.

Regarding claim 3, Chang ('562) discloses a gate polyoxide layer (Figure 5, item 24) with a thickness of about 50~100Å (col. 6, ln. 15-16). The claim language "...wherein the gate polyoxide layer prevents the silicon nitride layer from separating from the semiconductor substrate..." is functional language and not distinguishable over the prior art, because the polyoxide of Chang ('562) can perform the recited function.

Regarding claim 4, the claim language "wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800~900°C with the injection of oxygen" describes a product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. Therefore the structure of the instant polyoxide layer is not distinct from that of the disclosed oxide layer (Figure 5, item 24).

Regarding claim 5, Chang ('562) discloses that the silicon nitride layer has a thickness of about 100~500 Å (col. 6, ln. 26-30).

Regarding claim 6, the claim language "wherein the oxide layer is an oxide layer formed at a temperature of about 600~800°C using $SiCl_4$ and O_2" describes a product-by-process. Chang ('562) discloses an oxide film formed by LPCVD using TEOS, which is normally at a temperature around 700°C, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. Therefore the structure of the instant oxide layer is not distinct from that of the disclosed oxide layer (28).

Regarding claim 8, Chang ('562) discloses that the external spacer (Figure 5, item 30) is formed of silicon nitride (col. 6, ln. 39-40).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1, 2, 4, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figures in view of Chang et al. (US 6,358,864), hereafter "Chang" ('864).

Regarding claims 1 and 2, the applicant's prior art Figure 8 shows a semiconductor substrate (10) having a multi-layered spacer, comprising: a plurality of gate electrodes each including a gate oxide layer (15), a gate conductive layer (16), and a capping dielectric layer (17) formed on a semiconductor substrate; a gate polyoxide layer (19a) formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a predetermined portion of the semiconductor substrate, an oxide layer (20b) and an external spacer (22a). The prior art also discloses in Figure 8

a pad (28) formed in a region between adjacent gate electrodes having the multi-layered spacer and being in contact with the semiconductor substrate; and an interlevel dielectric layer (30) formed on the pad and each gate electrode having the multi-layered spacer.

The prior art does not disclose a silicon nitride layer being in contact with the sidewalls of the capping dielectric layer and the gate polyoxide layer, nor does it disclose the oxide layer (20b) being in contact with the silicon nitride layer. The end result of the prior art is a sidewall spacer with an oxide/oxide/nitride (OON) structure.

Chang ('864) teaches a method of fabricating an oxide/nitride/oxide/nitride (ONON) multilayer structure. In column 4, on lines 18-21, Chang ('864) discloses that his method could be applied at the process of forming a multilayer spacer, such as an ONON.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the prior art with the method taught by Chang ('864) to arrive at a multilayered-spacer semiconductor structure, simply by inserting a nitride layer between the existing oxide layers. Motivation to do so would include the desirability of the following: enhancement of the resistivity strength of the dielectric film (col. 1, ln. 20), isolation of the silicon nitride layer from the silicon substrate in order to avoid degradation of the substrate, use of the first nitride layer as an etch stop to further protect the substrate, improved control tolerances of the gate electrode length, and a better shape for the sidewalls whereby source/drain contact areas are more reliable.

Regarding claim 4, the claim language "wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800~900°C with the injection of oxygen" describes a product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Chang ('864) discloses an oxide layer formed at a temperature of 750-850°C with the injection of N_2O.

Regarding claim 6, the claim language "wherein the oxide layer is an oxide layer formed at a temperature of about 600~800°C using $SiCl_4$ and O_2" describes a product-by-process. Chang ('864) discloses an oxide film formed by LPCVD at a temperature of 750-850°C using N_2O and SiH_2Cl_2, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant oxide layer is not distinct from that of the disclosed oxide layer.

Regarding claim 8, Chang ('864) discloses that the external spacer is formed of silicon nitride (col. 4, ln. 18-20).

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over each of Divakaruni, Takahashi, Chang ('562) and Chang ('864). While all of the disclosures by Divakaruni, Takahashi, Chang ('864) and Chang ('562) teach the claimed oxide layer, none teach the specific process or thickness as claimed.

The claim language "wherein the oxide layer is a middle temperature oxide layer or a high temperature oxide layer having a dielectric constant of 3.9..." describes a

product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps, therefore the instant structure is not distinct from the structures disclosed by Divakaruni, Takahashi, Chang ('562) and Chang ('864).

With regard to the thickness of the oxide layer, "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). See also the case of *In re Huang*, 40 USPQ2d 1685 (Fed. Cir. 1996), in particular the passage "Accordingly, one of ordinary skill would have experimented with various thicknesses to obtain an optimum range."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-1705. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jci

GEORGE ECKERT
PRIMARY EXAMINER